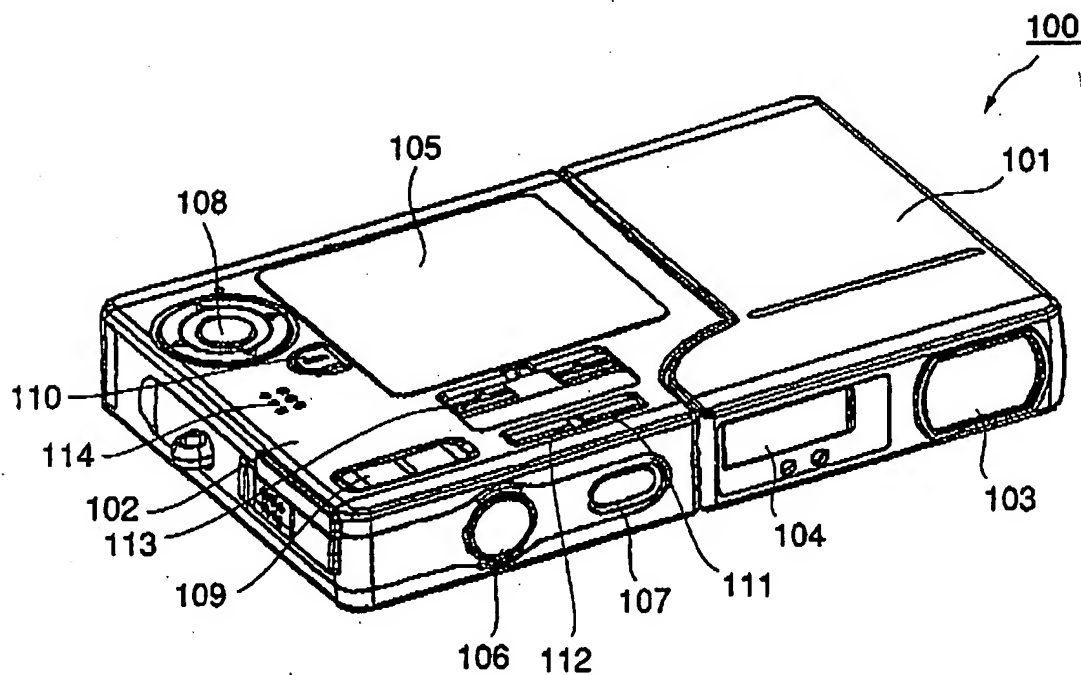


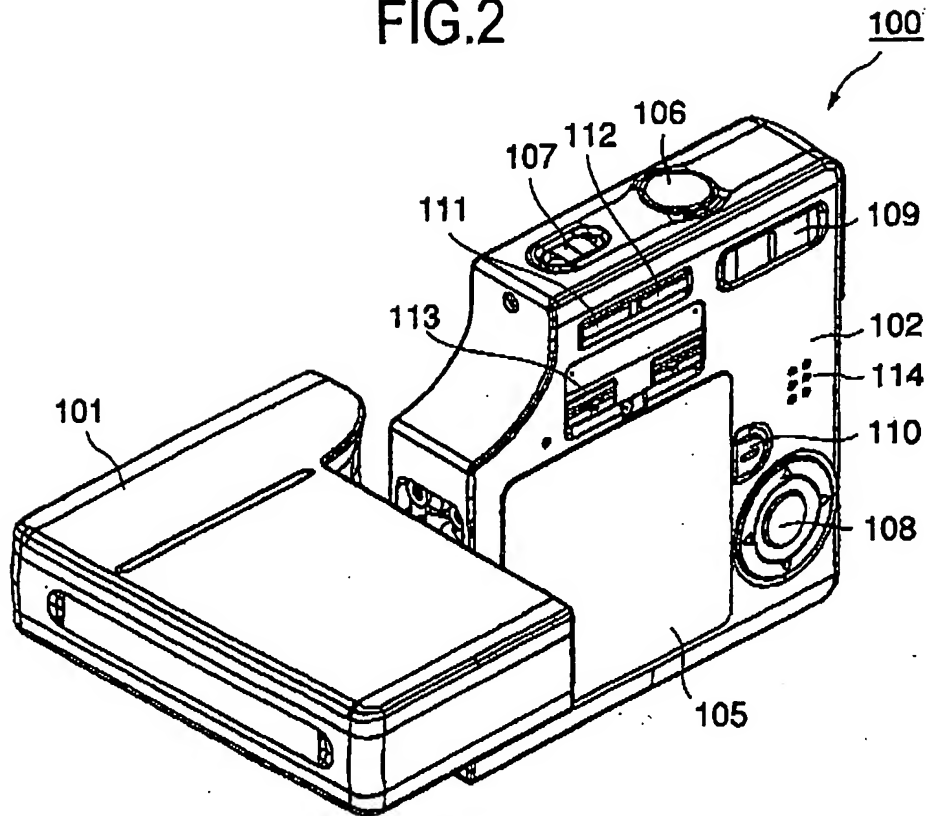
1 / 41

FIG.1



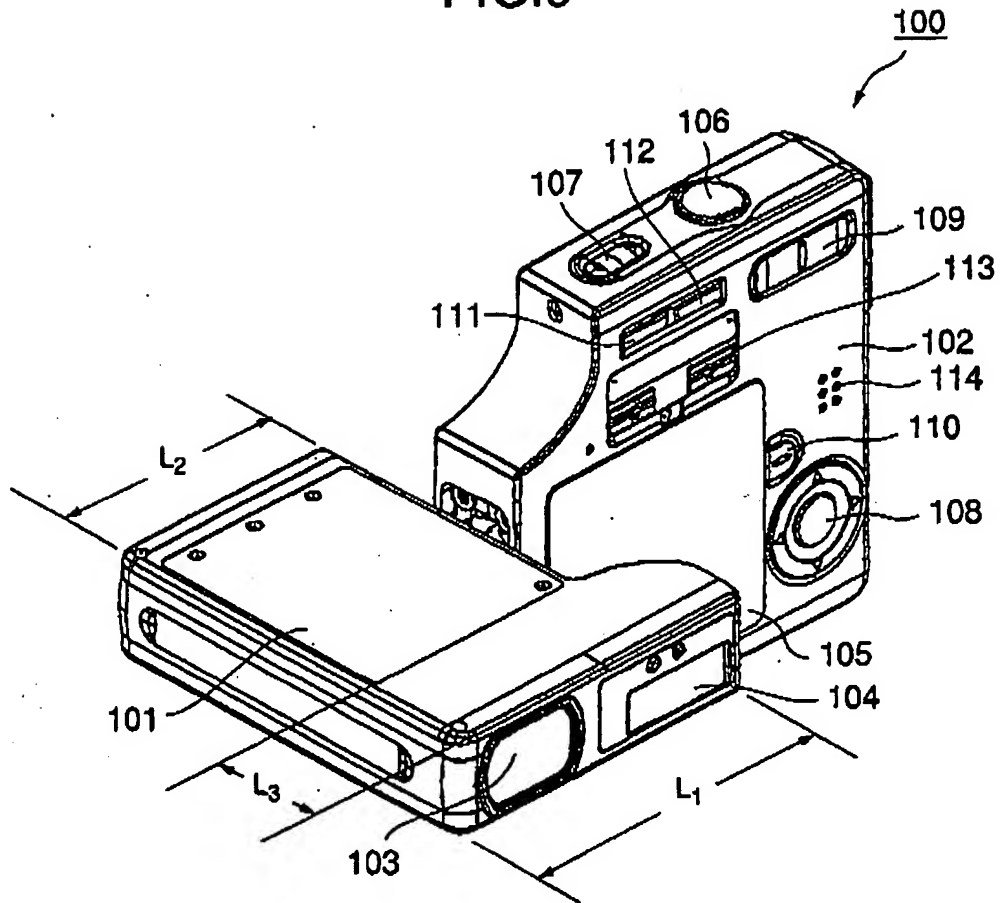
2 / 41

FIG.2



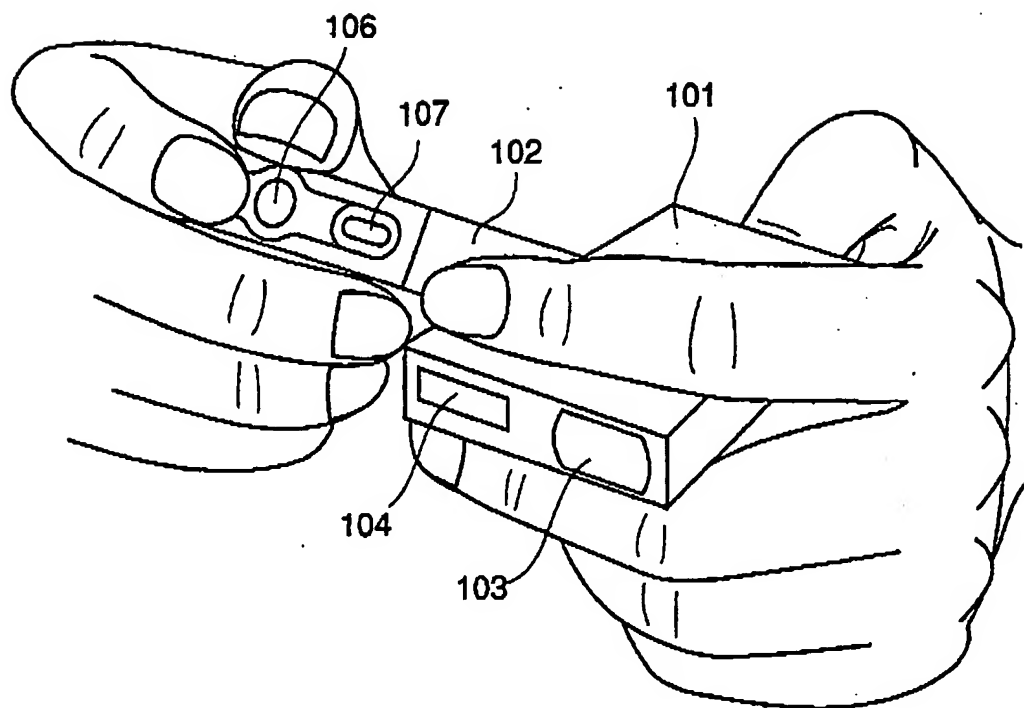
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FIG.3

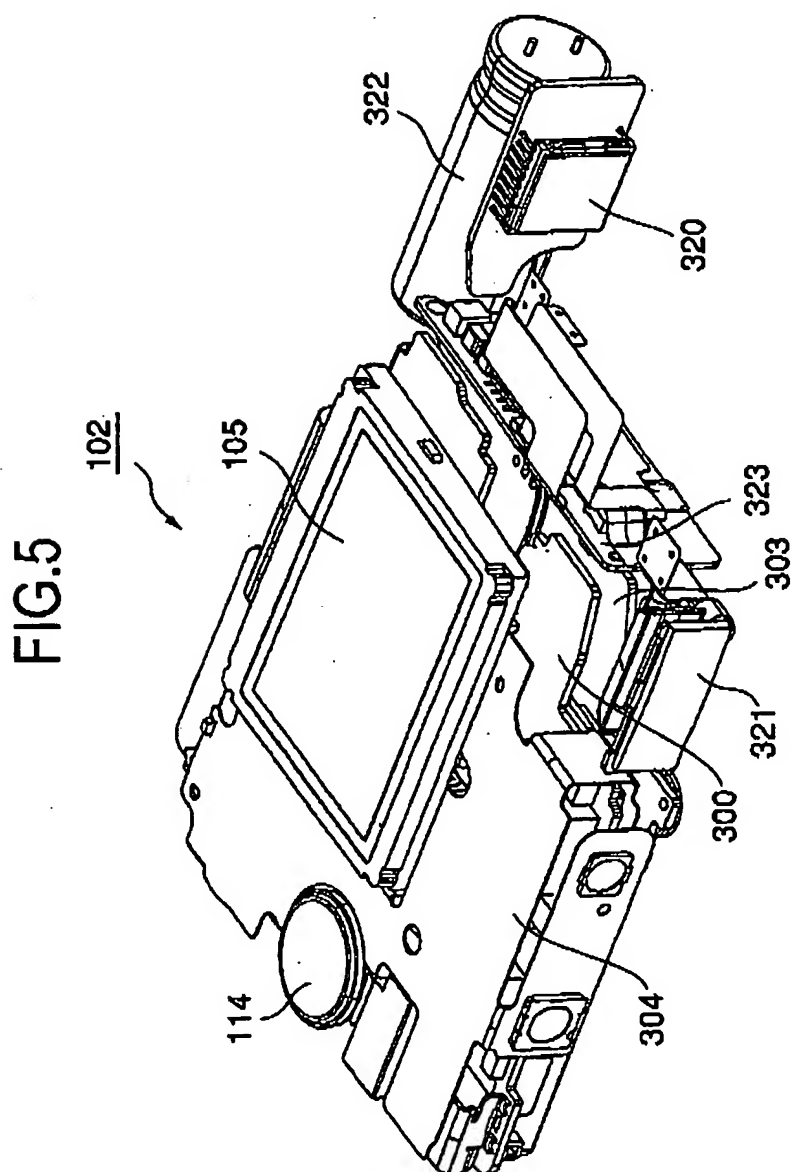


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FIG.4



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FIG.6(B)

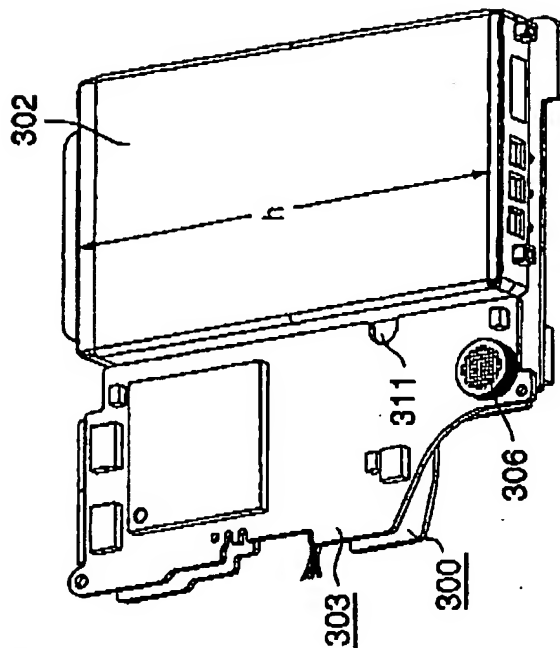
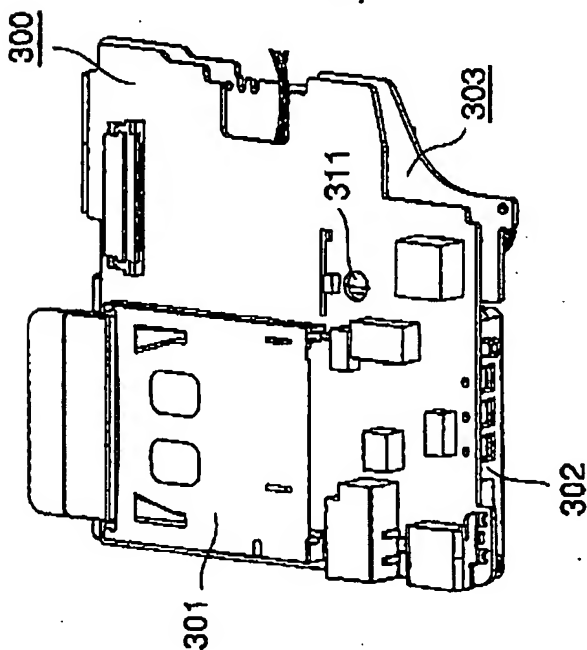


FIG.6(A)



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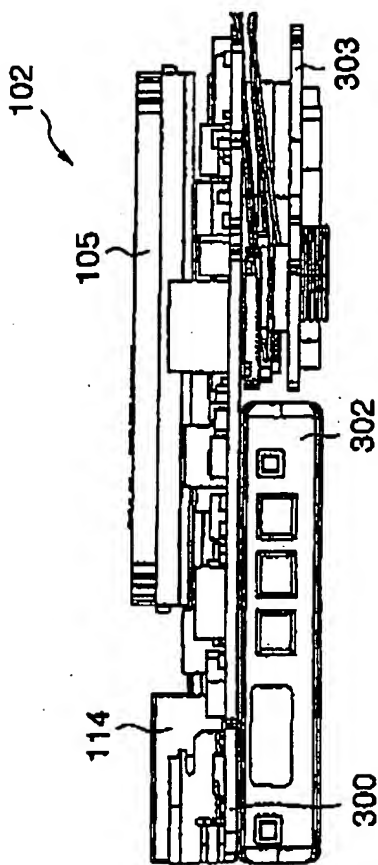


FIG. 7(A)

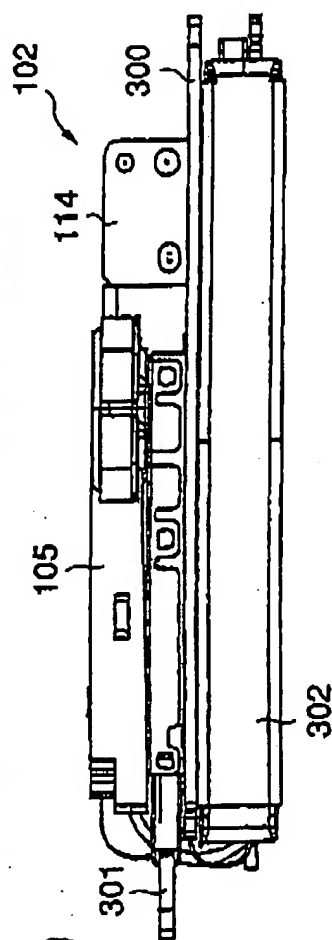


FIG. 7(B)

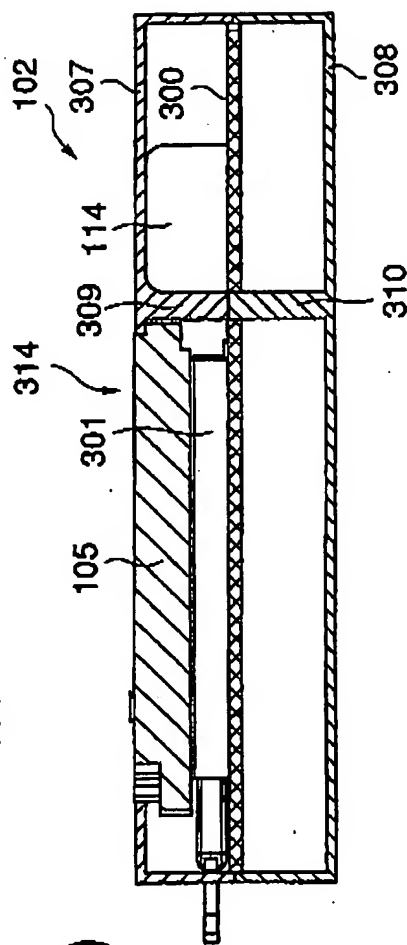
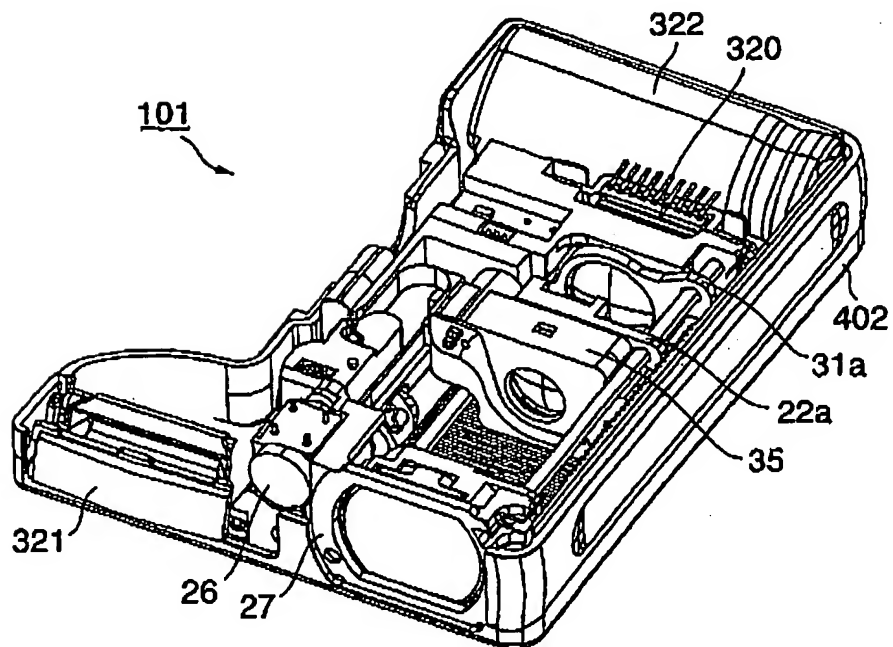


FIG. 7(C)

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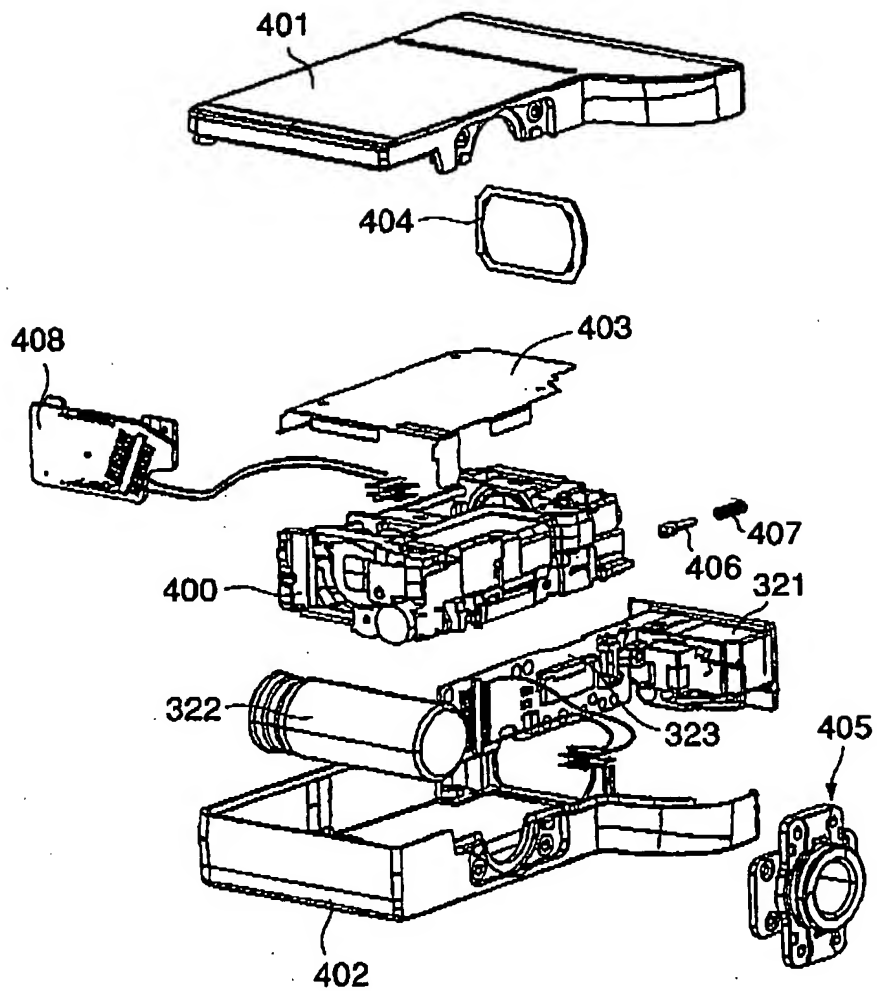
FIG.8



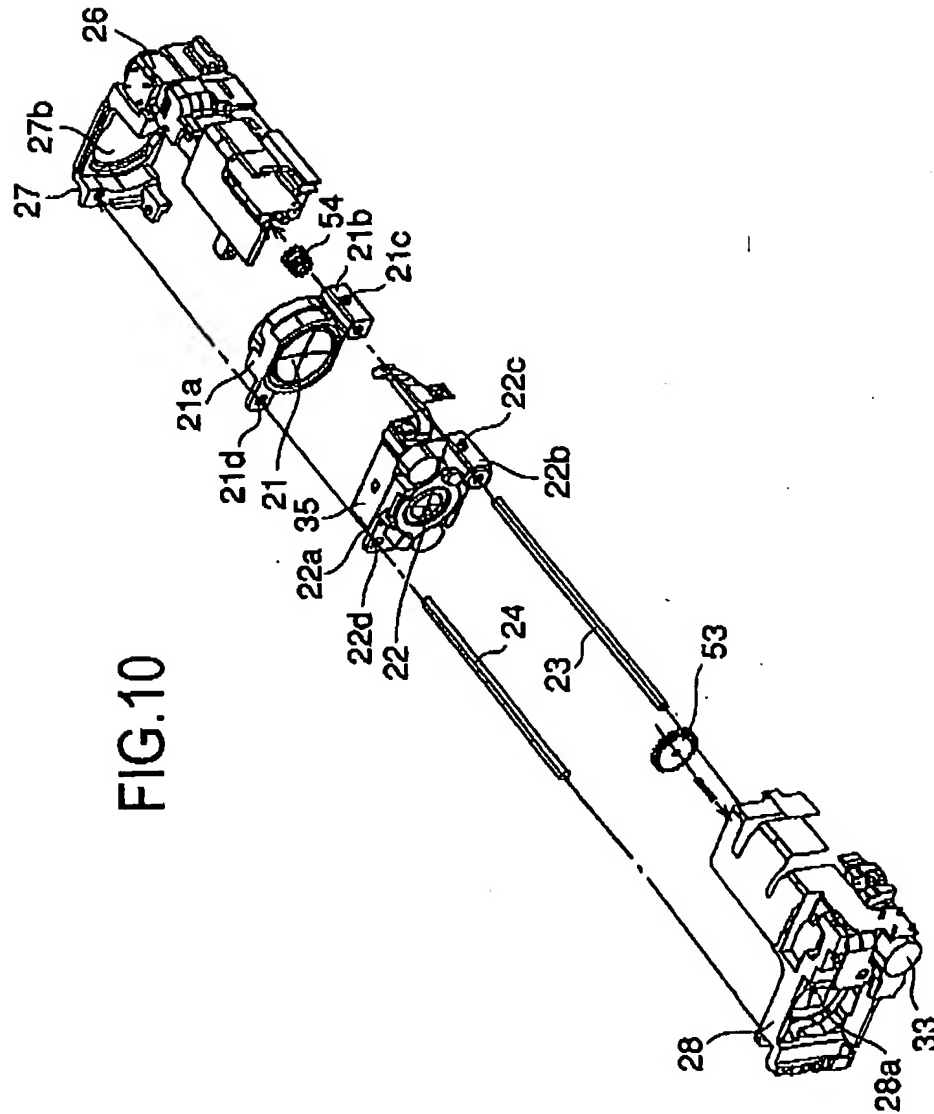


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FIG.9

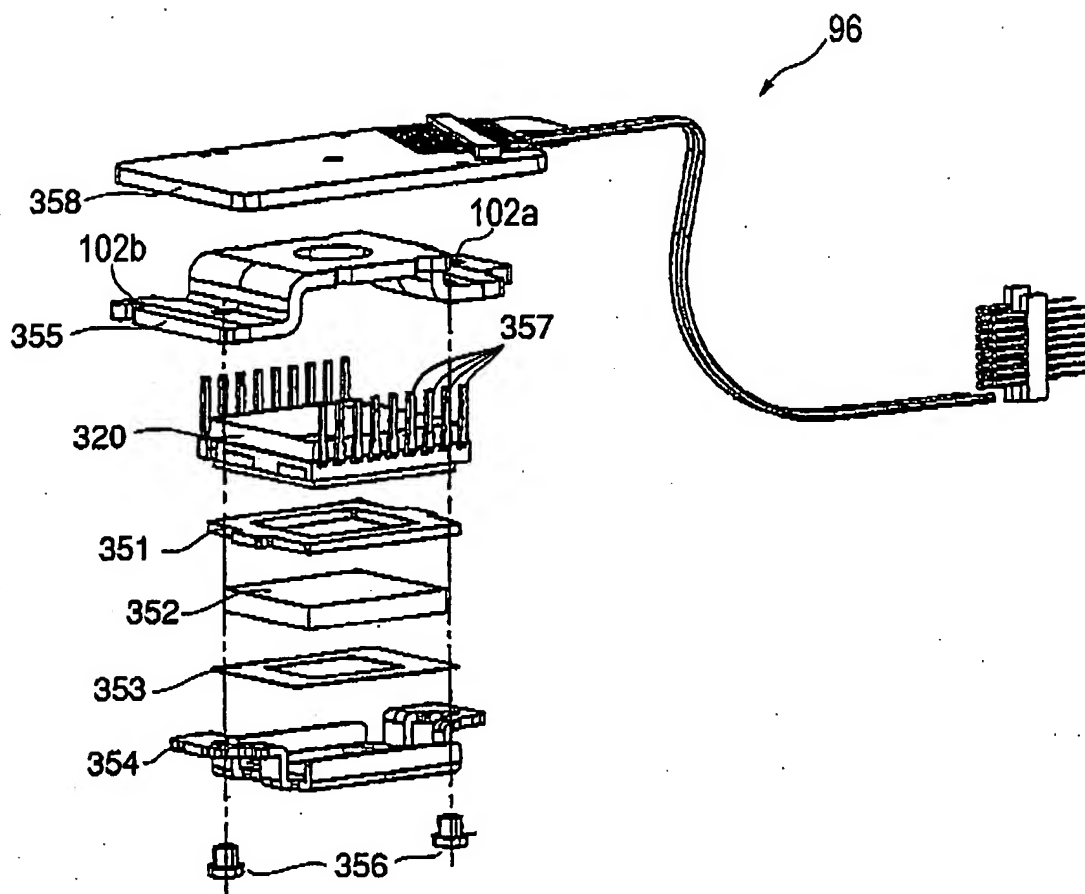


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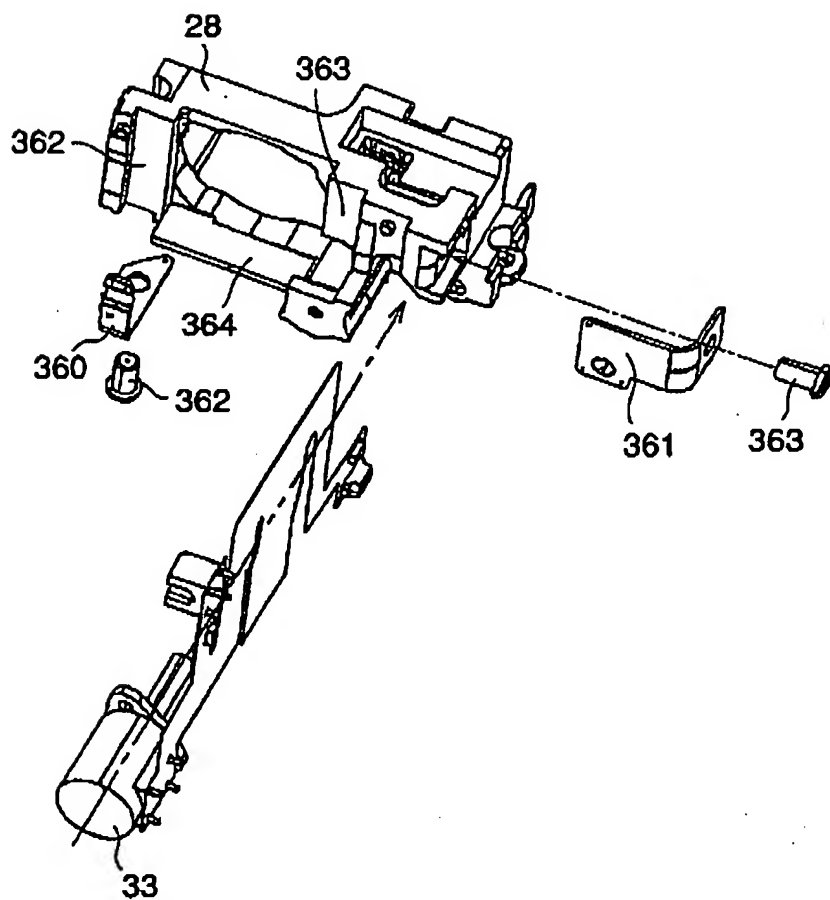
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FIG.11



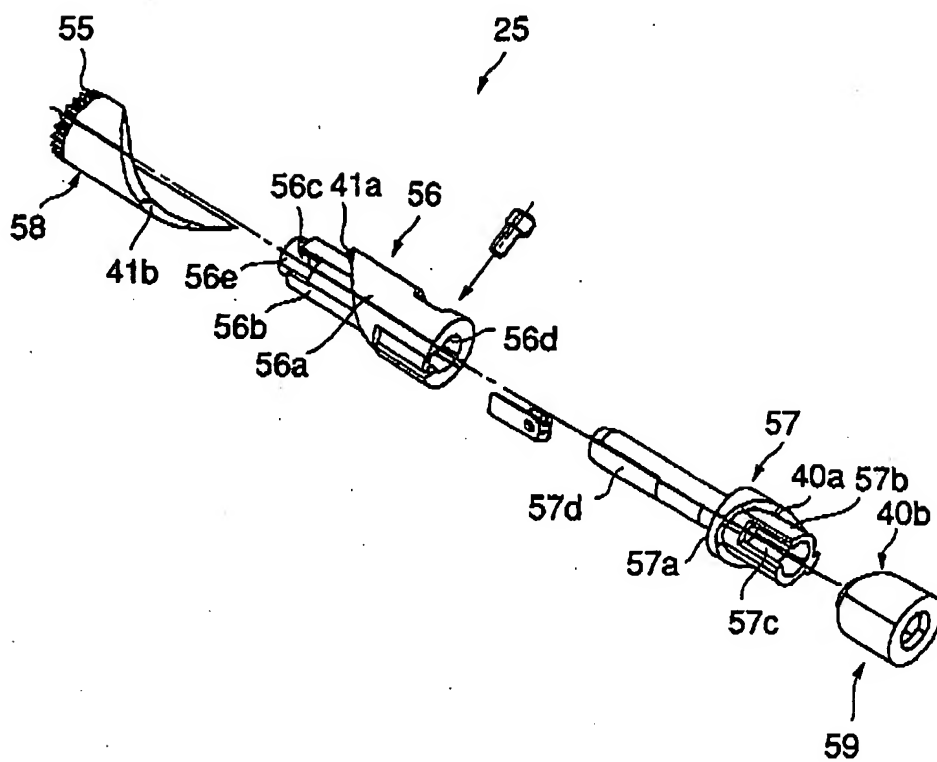
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FIG.12



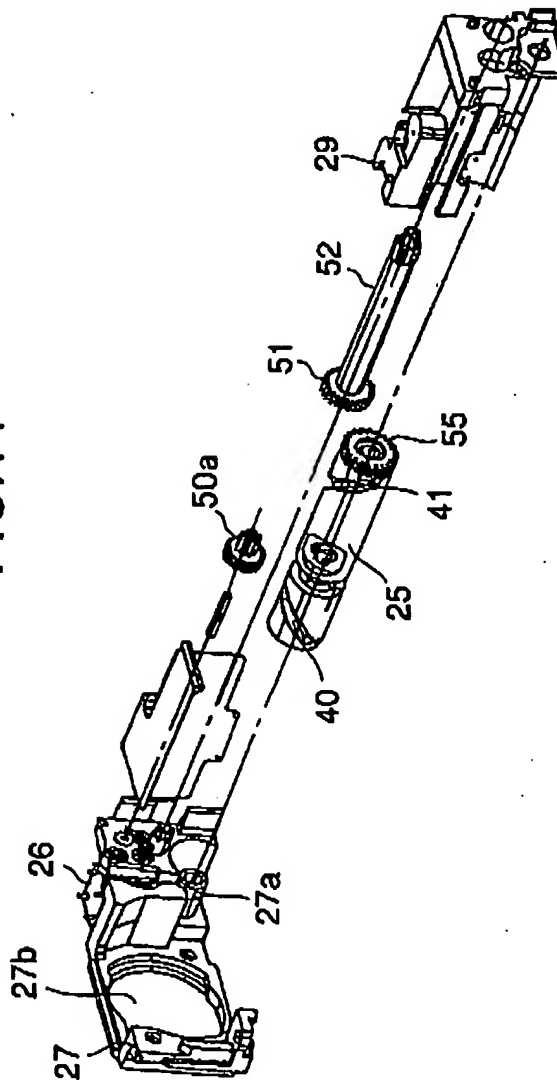
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FIG.13



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FIG.14



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FIG.15

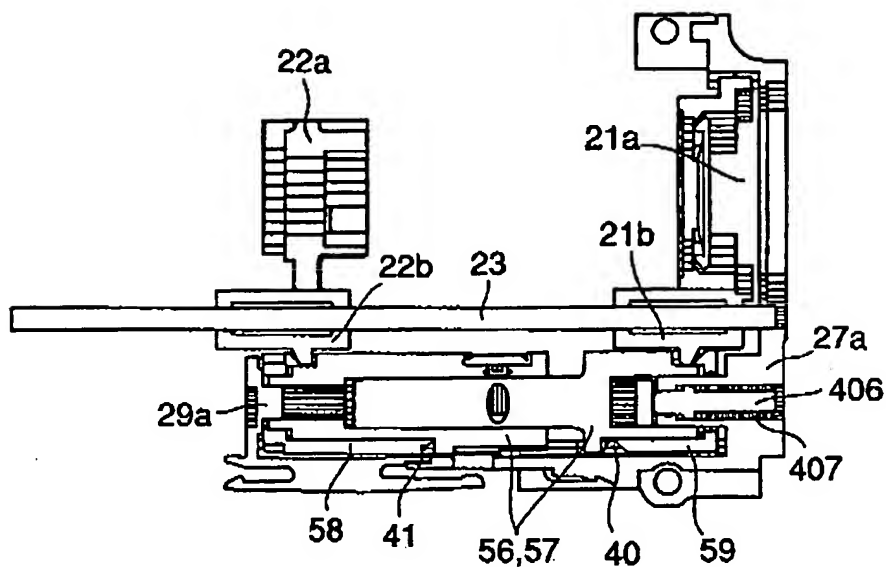
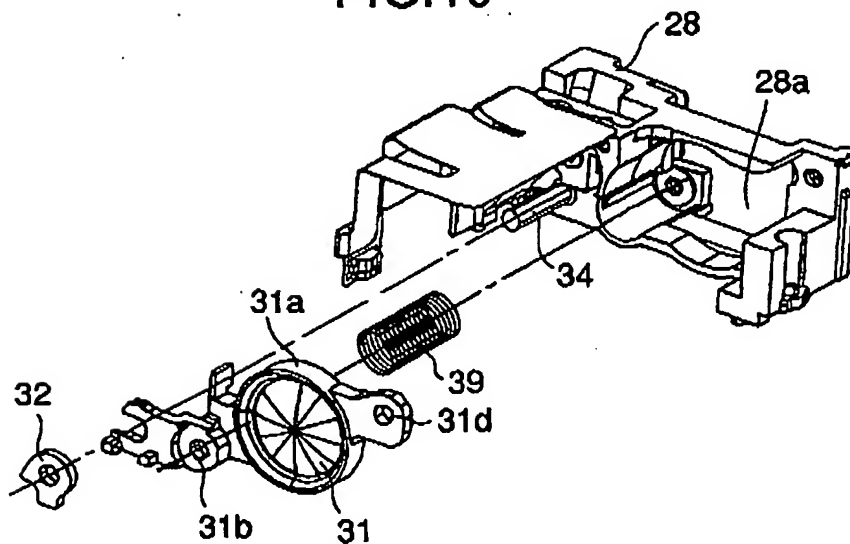
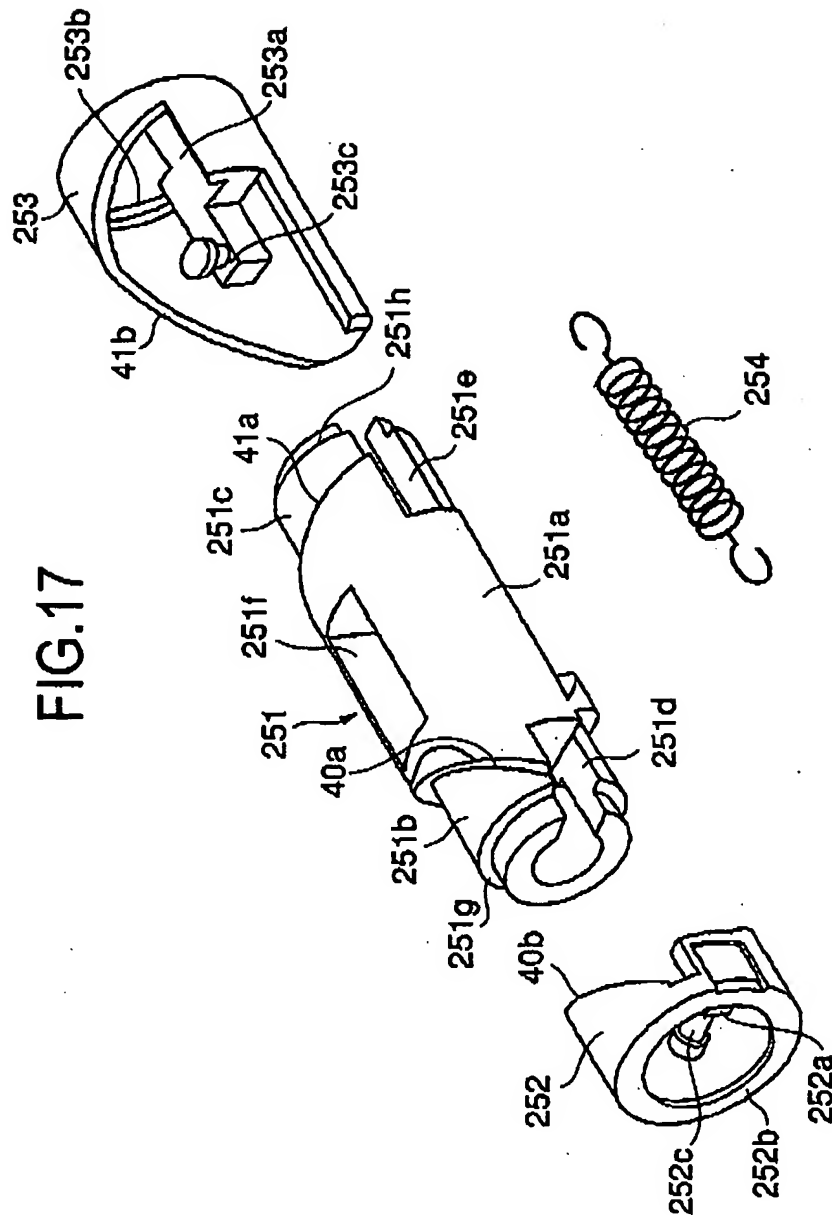


FIG.16



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FIG.18

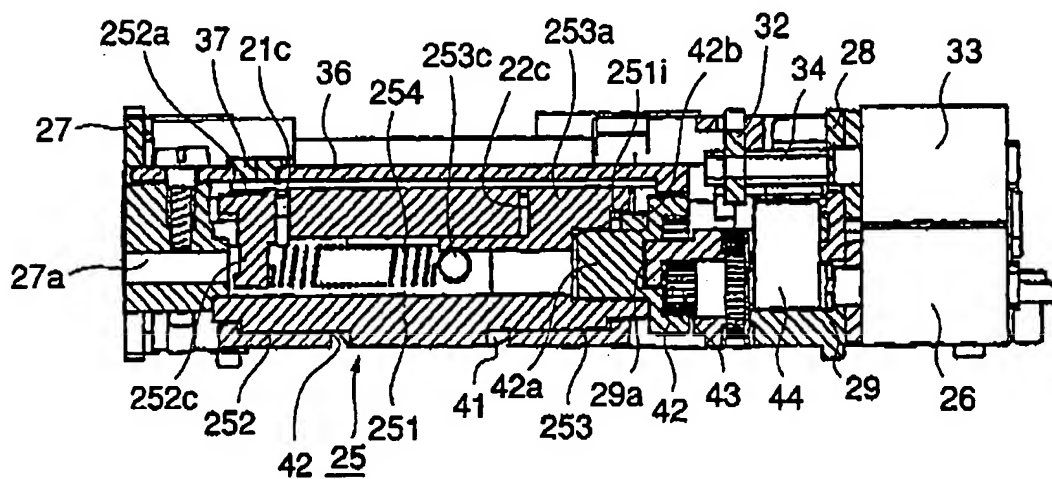
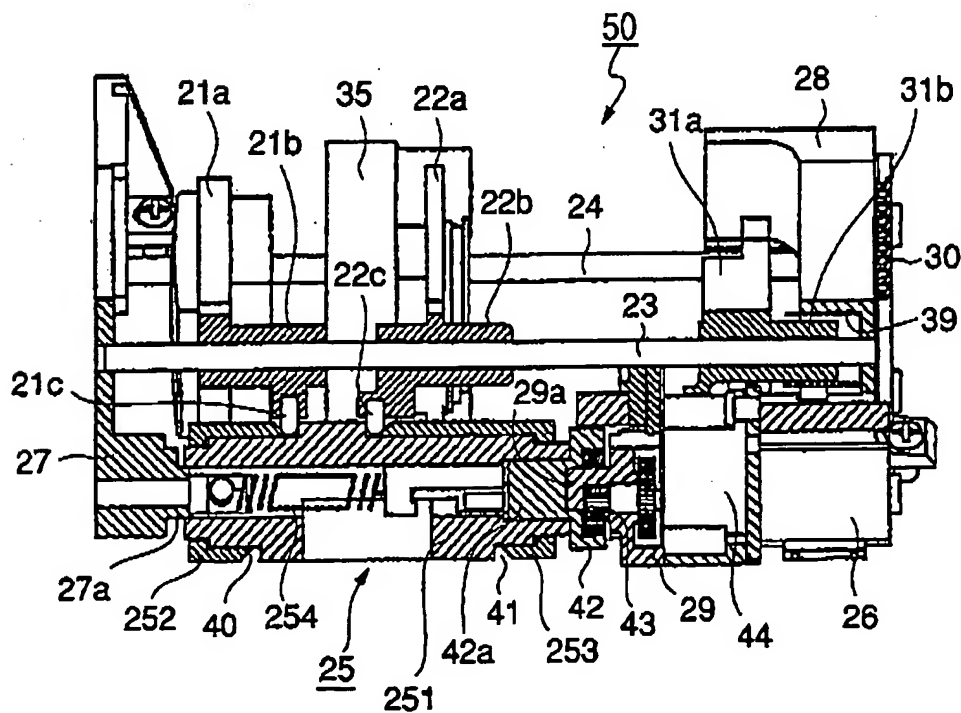


FIG.19



This cross-sectional diagram illustrates a semiconductor device with two transistors. A central channel layer (40) is positioned between two gate structures (21c and 22c). The gate structures are formed by a stack of layers including a gate oxide (23), a gate dielectric (21d or 22d), and a gate electrode (21b or 22b). The channel layer (40) is doped with impurities (F1) to form source regions (40a) and drain regions (40b). The device is mounted on a substrate (25) which contains a base layer (251) and a passivation layer (252).

FIG.21(A)

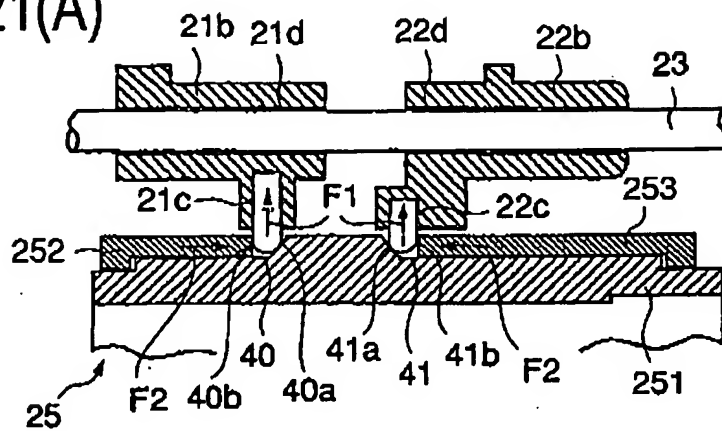


FIG.21(B)

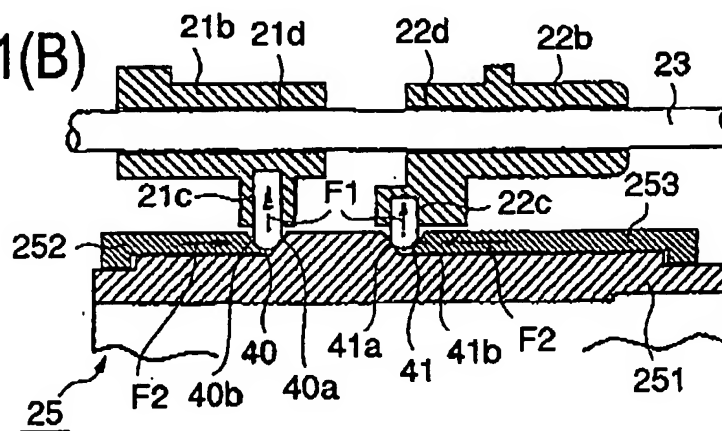
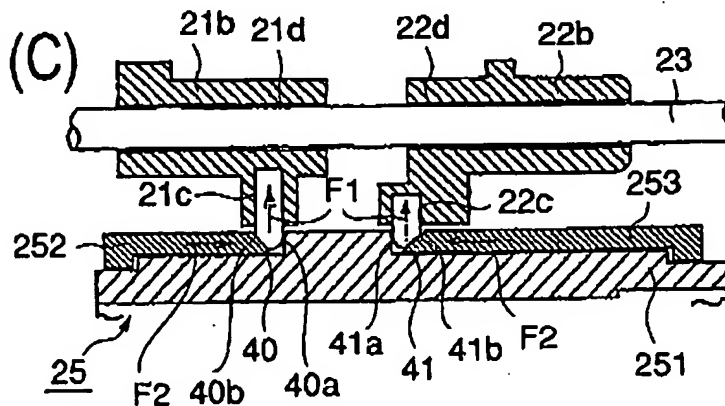


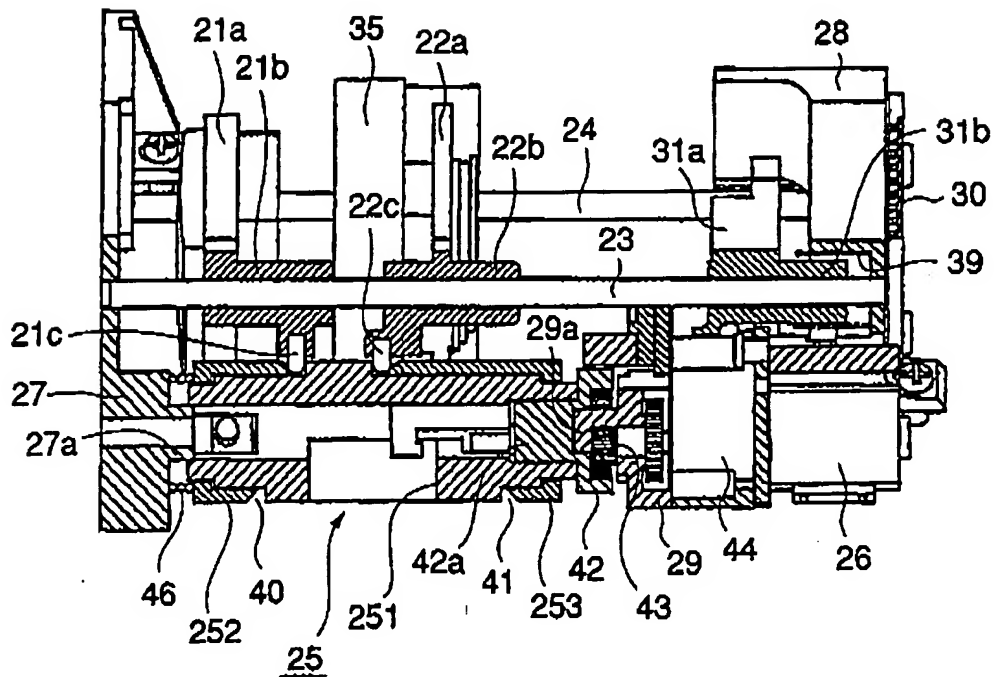
FIG.21(C)





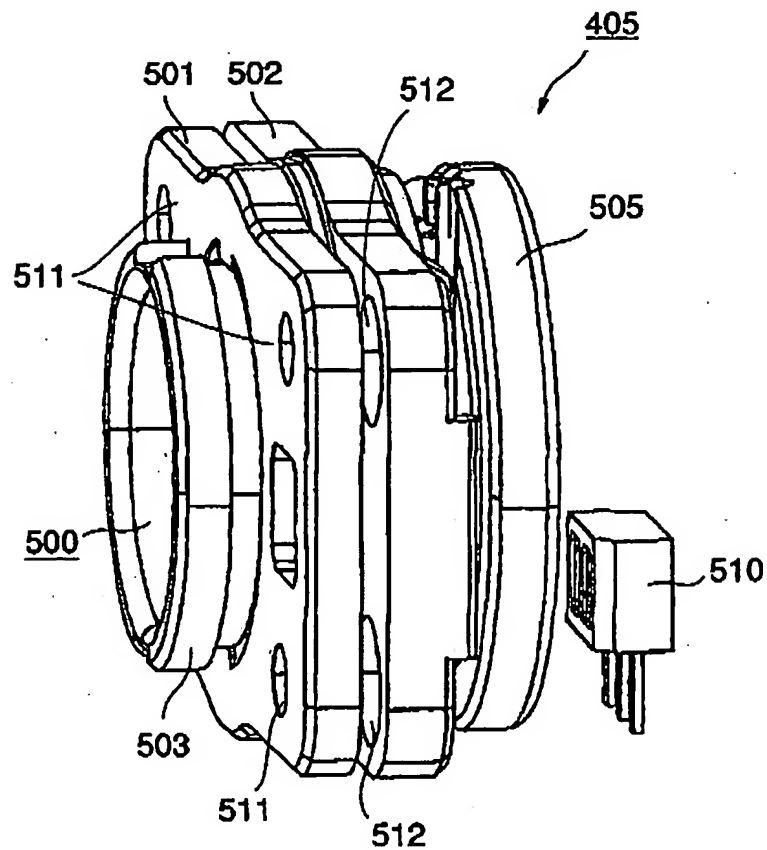
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FIG.23

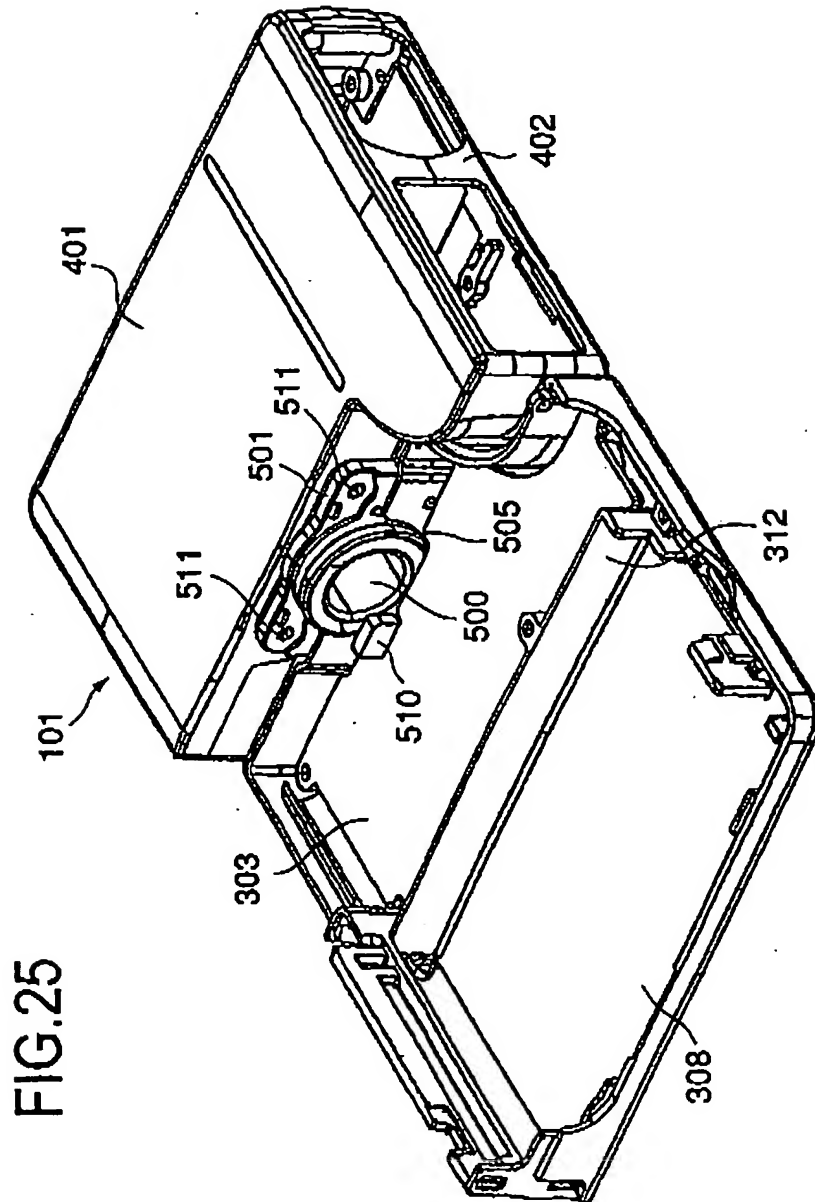


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FIG.24

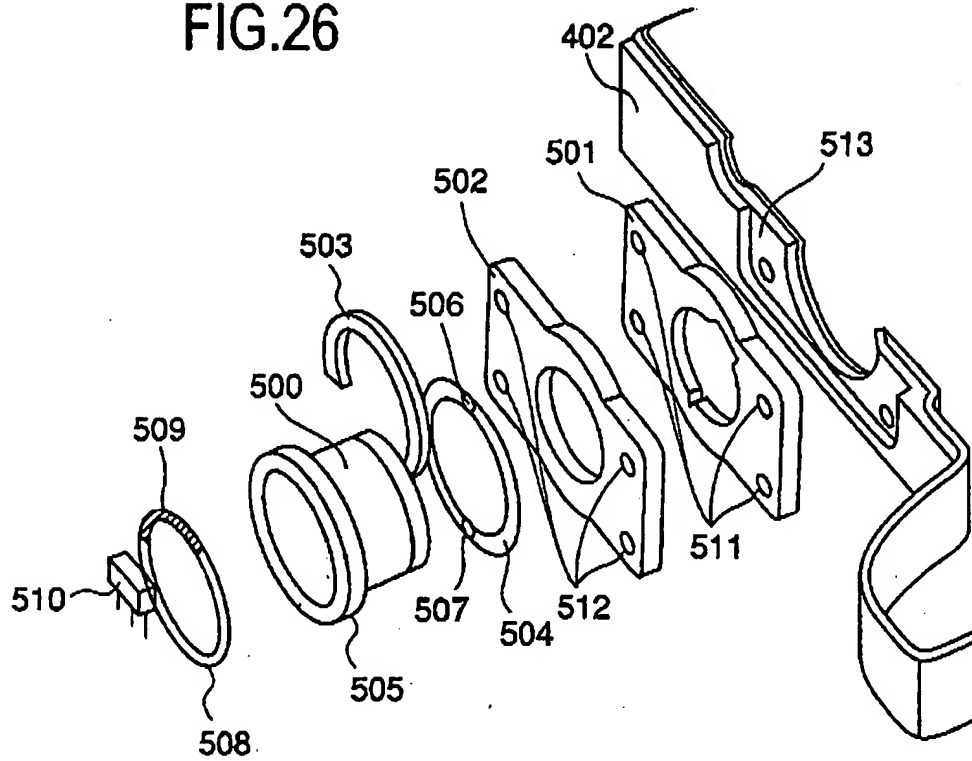


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FIG.26





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FIG.27

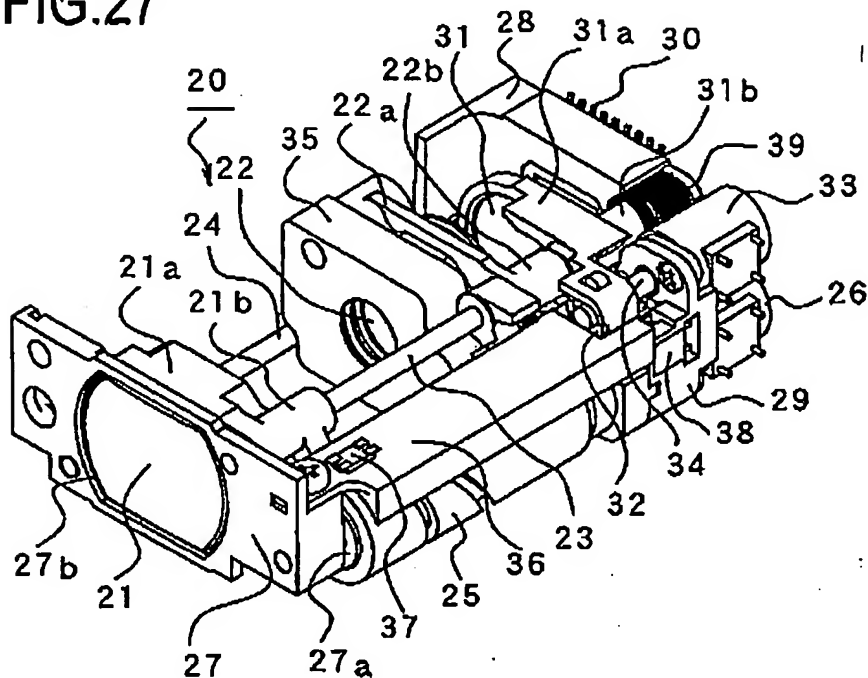
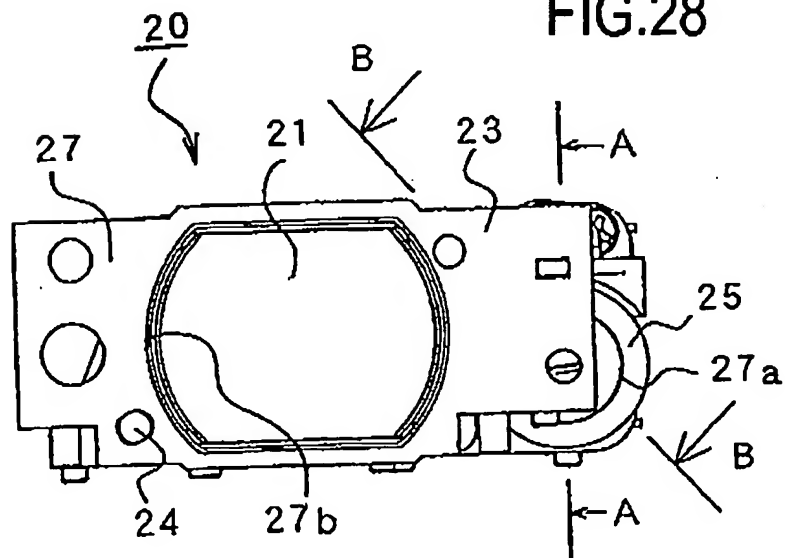


FIG.28



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FIG.29

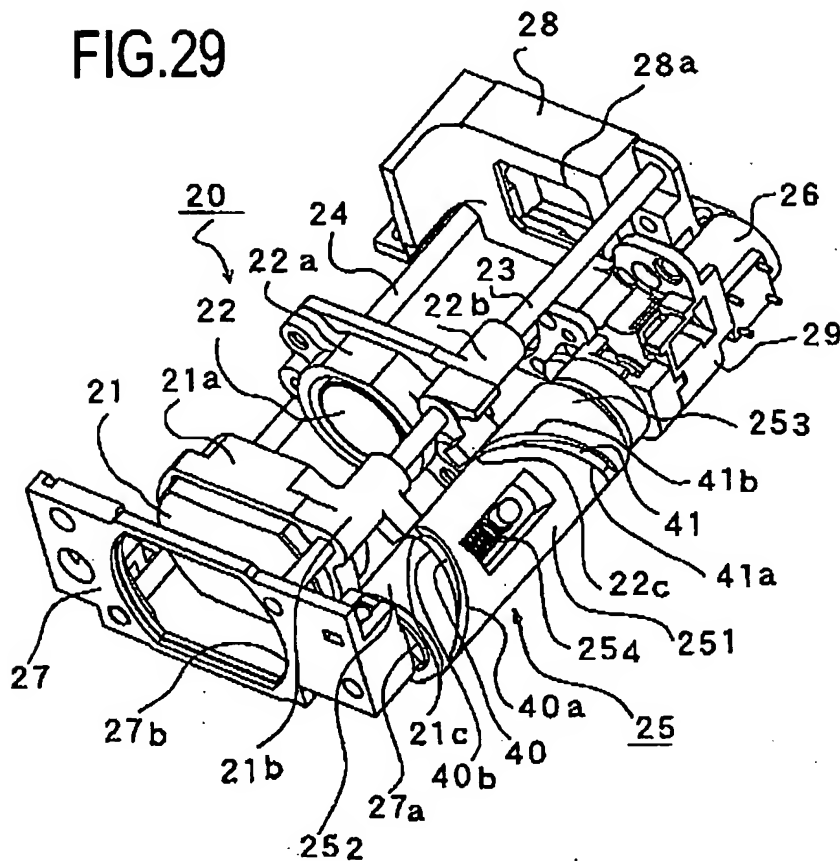
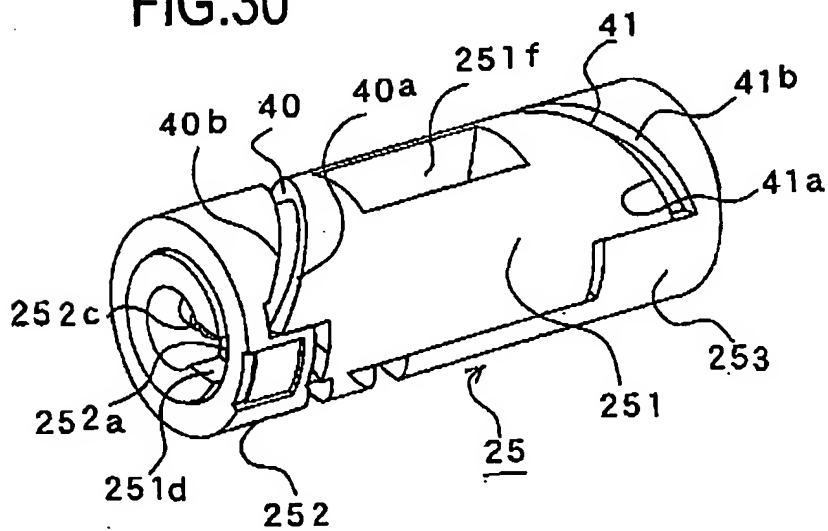
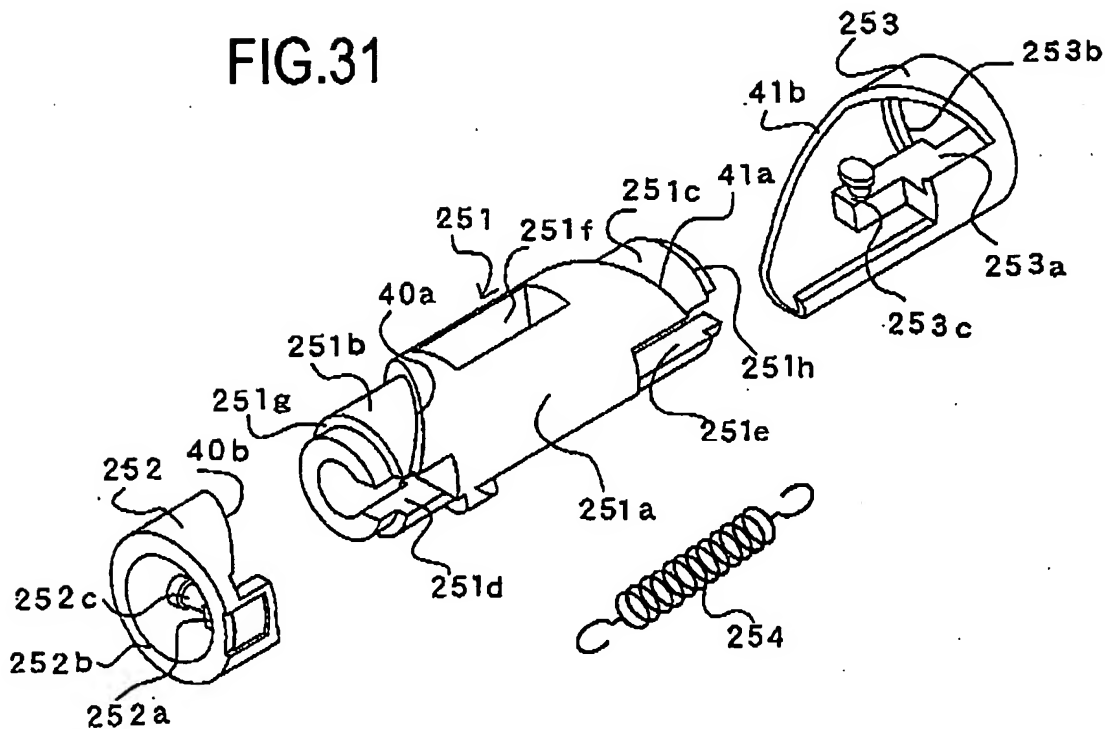


FIG.30



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FIG.31



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FIG.32

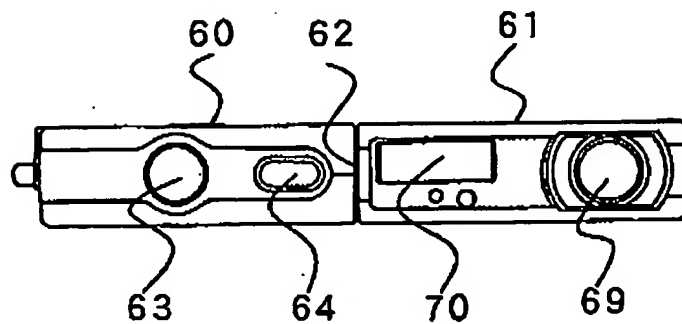
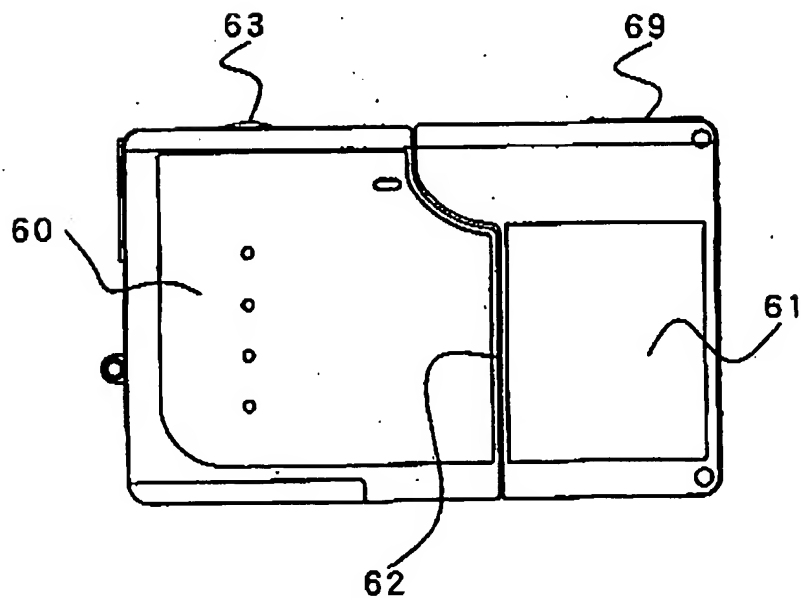


FIG.33



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FIG.34

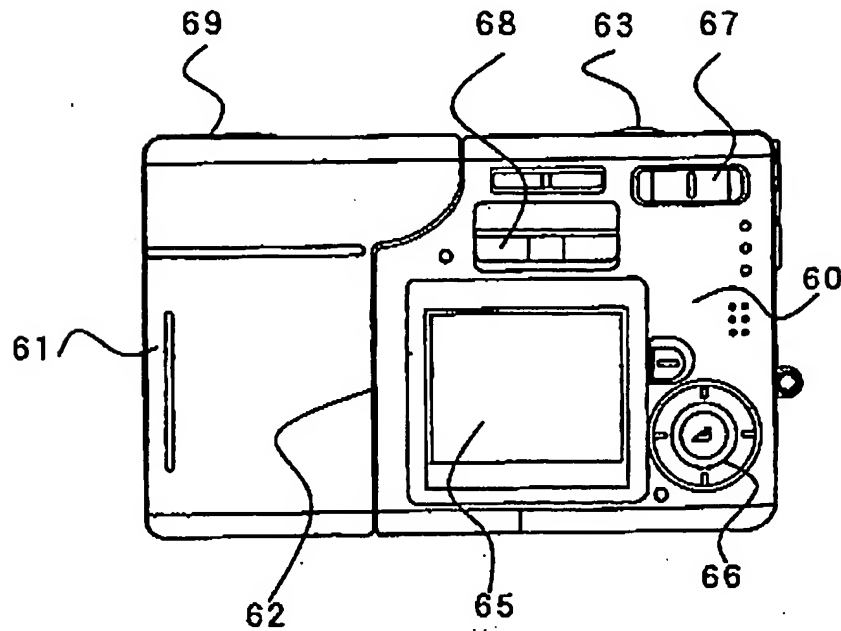
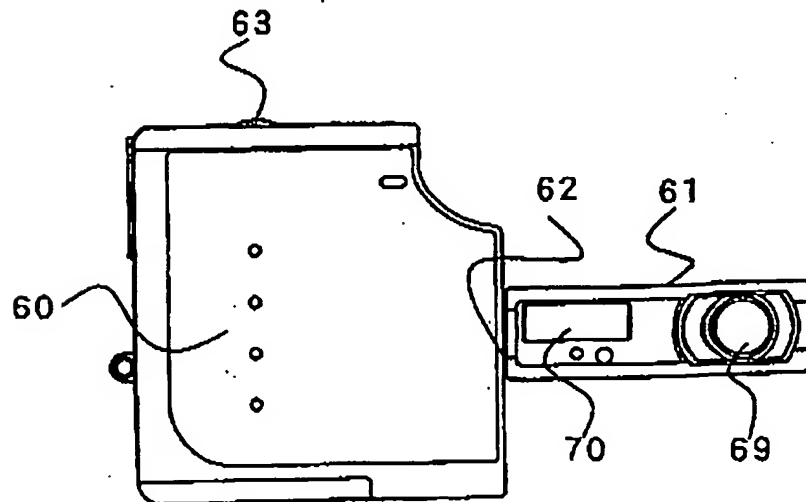
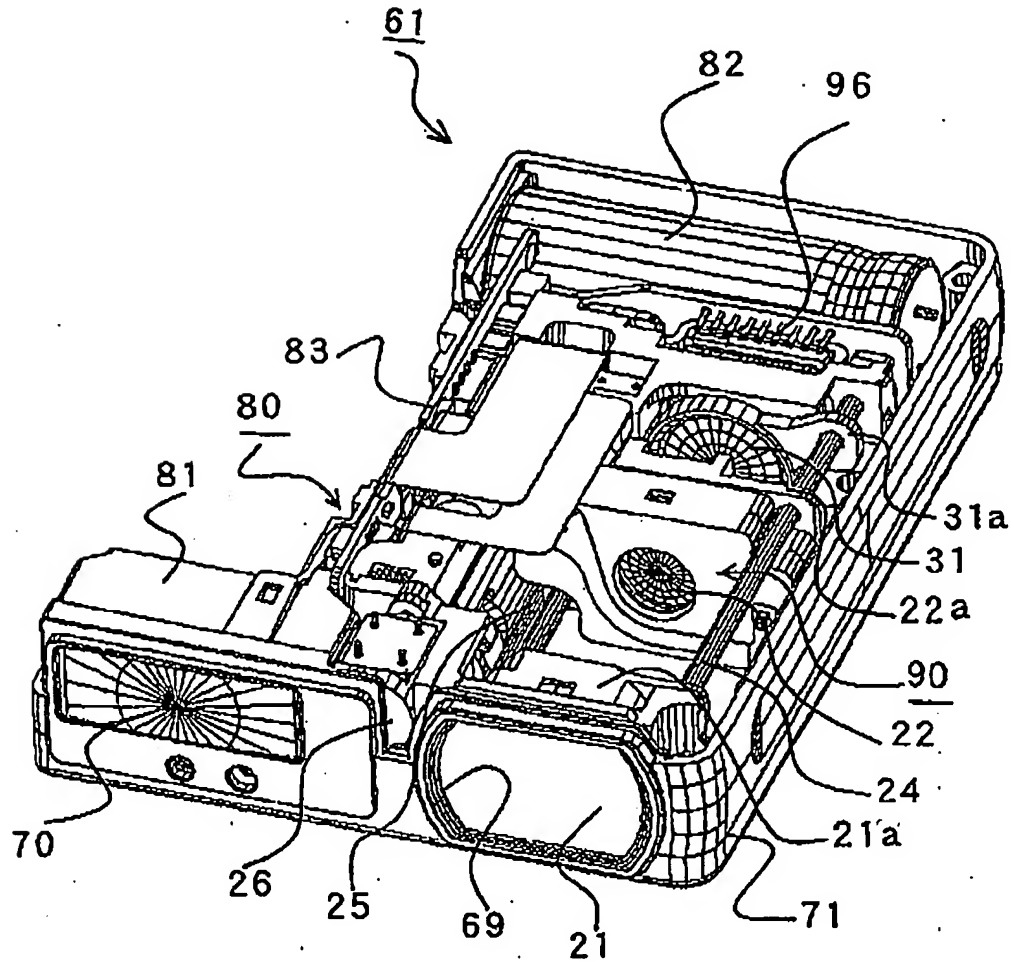


FIG.35



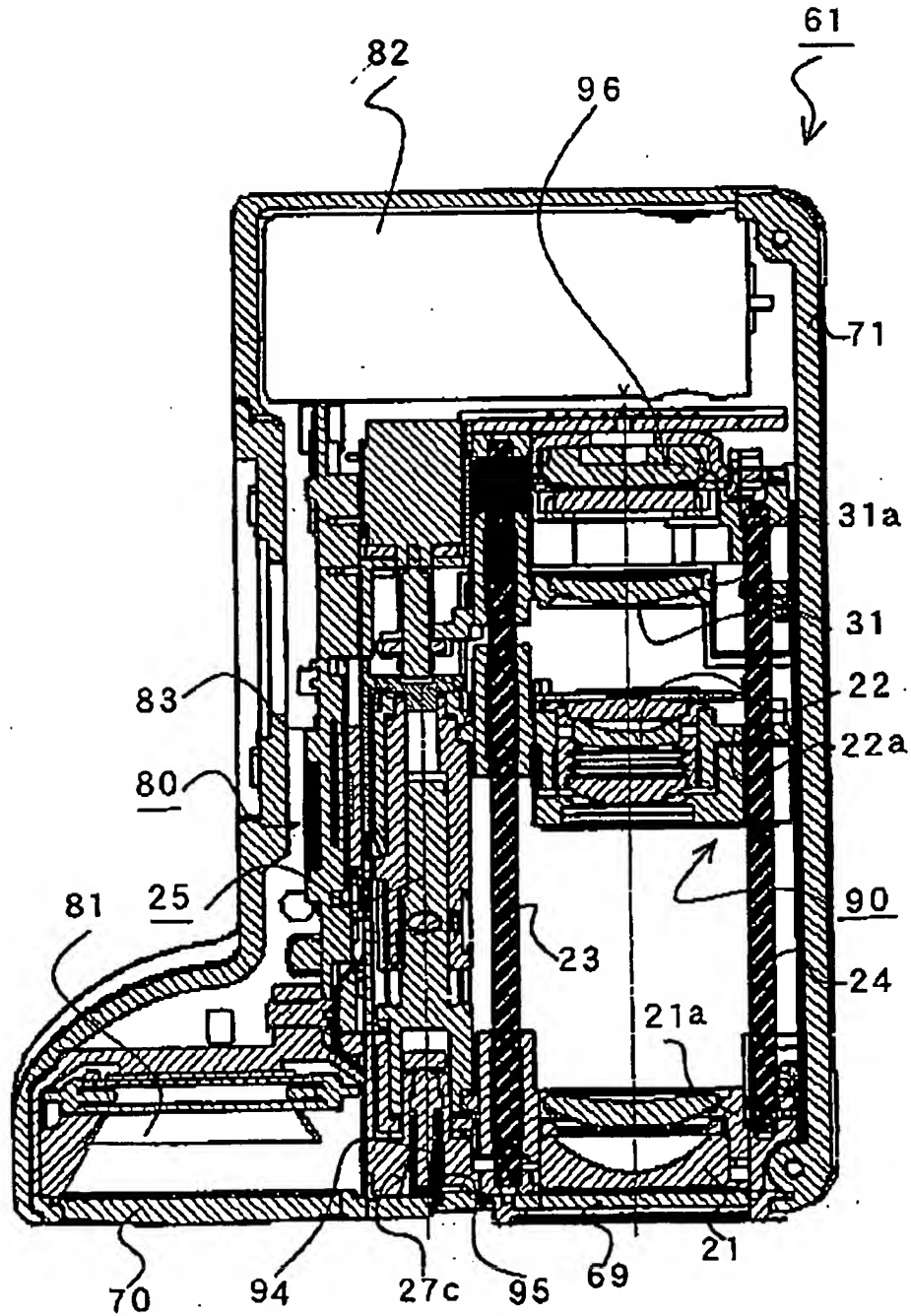
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FIG.36



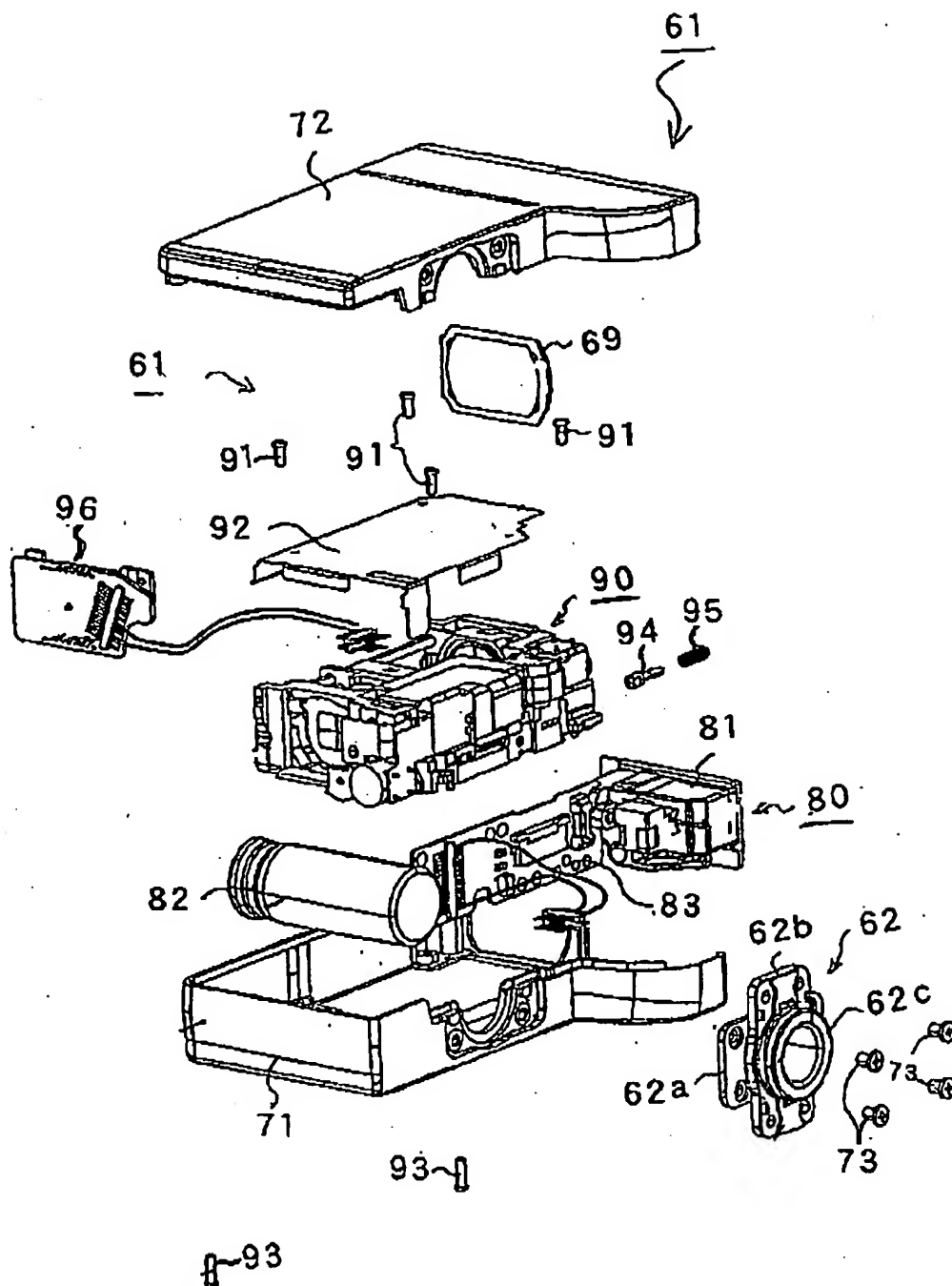
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FIG.37



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FIG.38





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FIG.39

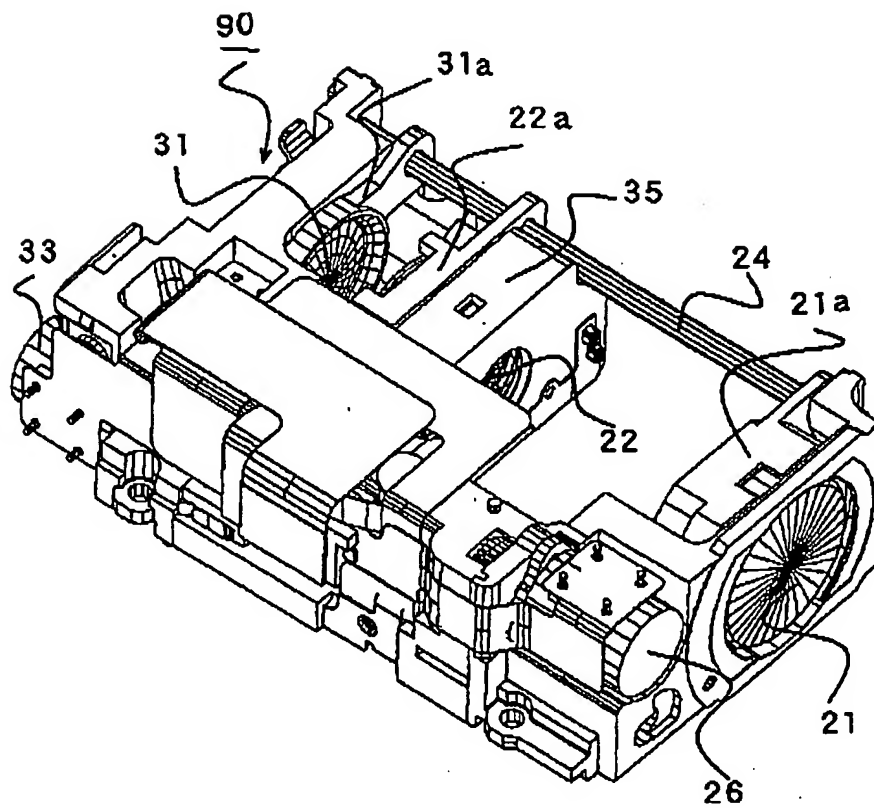
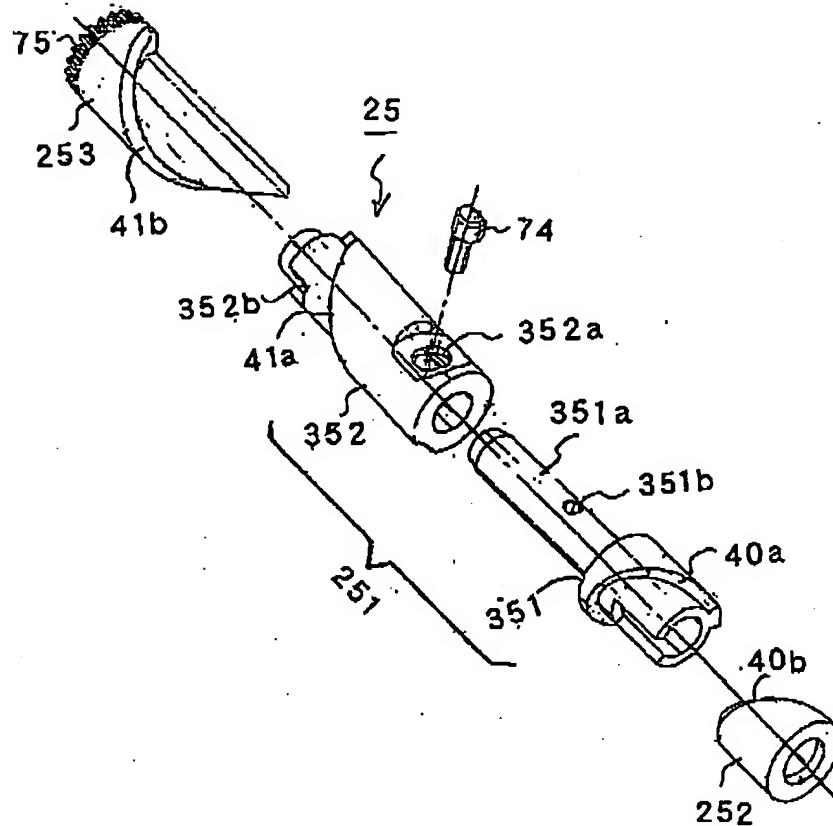
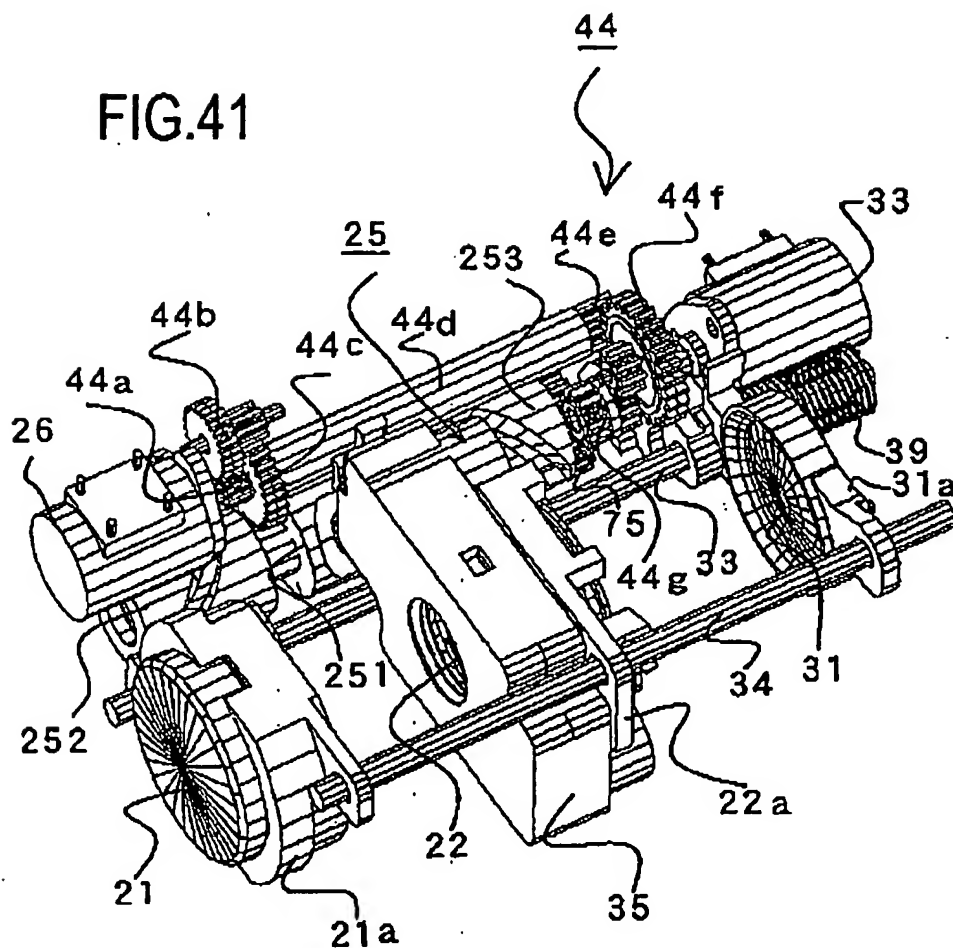


FIG.40



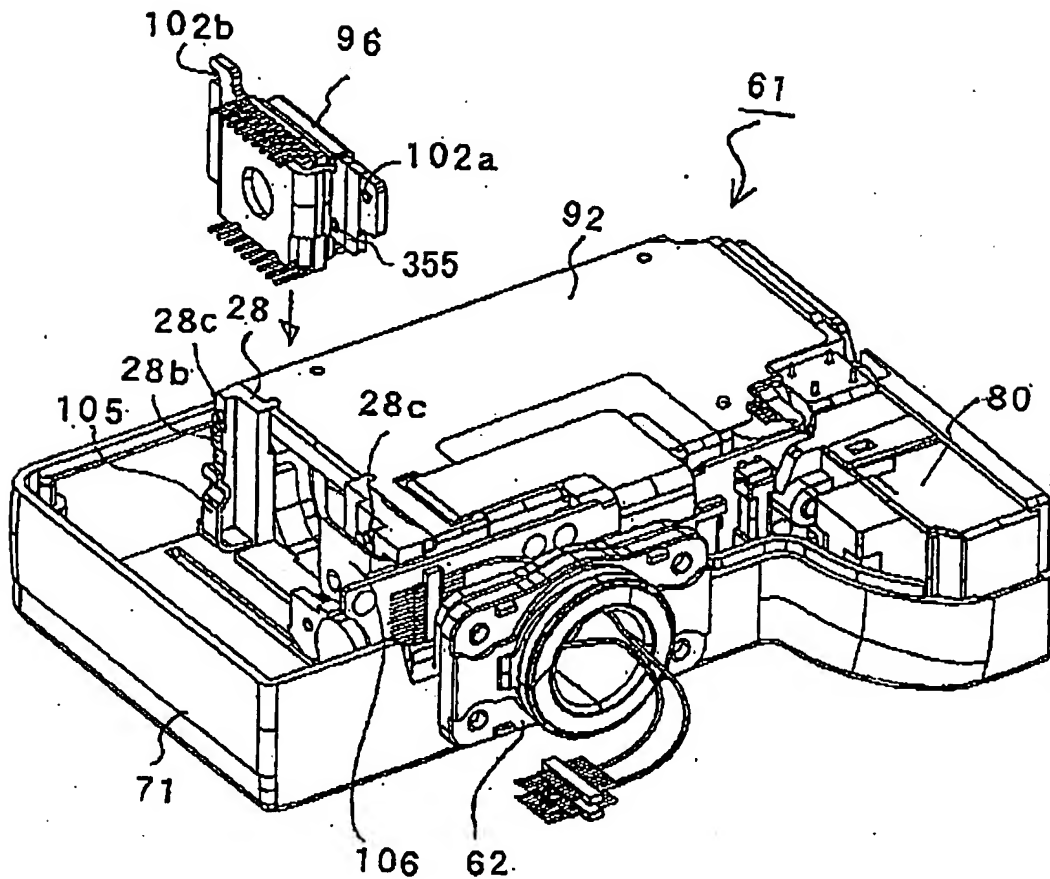
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FIG.41



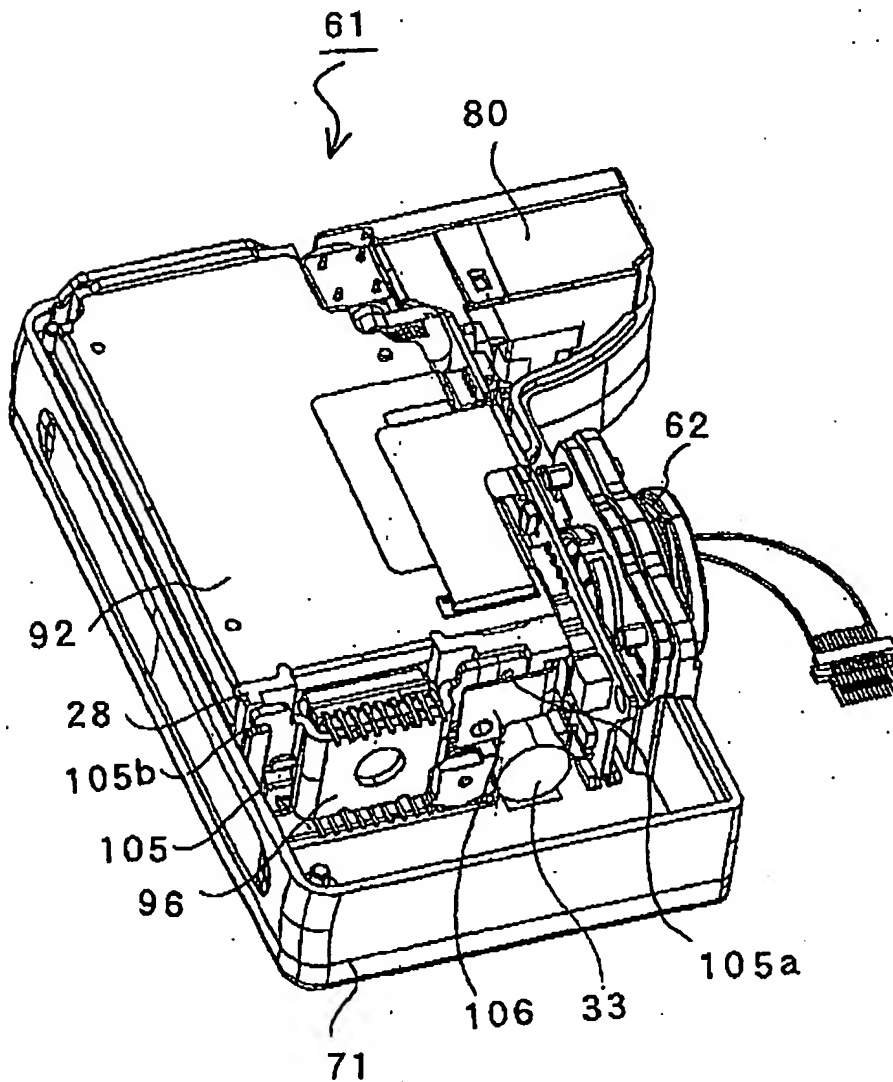
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FIG.42



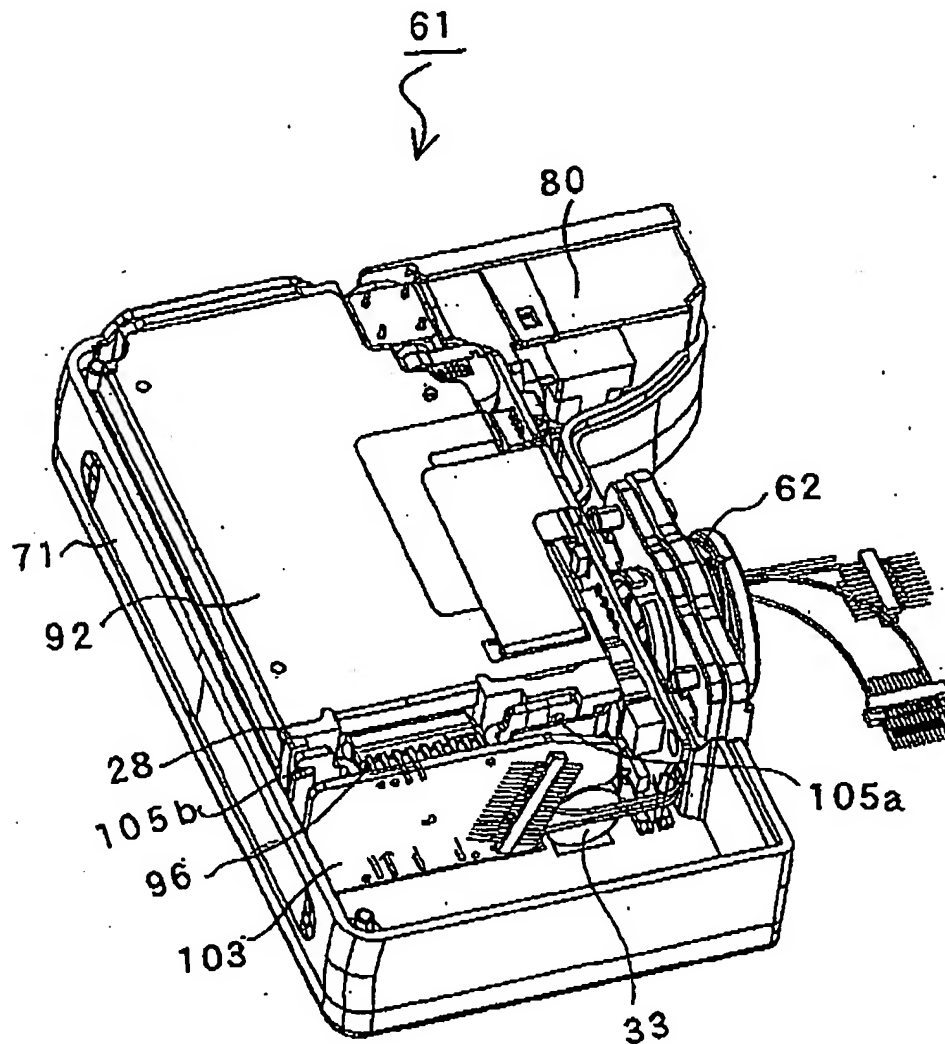
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FIG.43



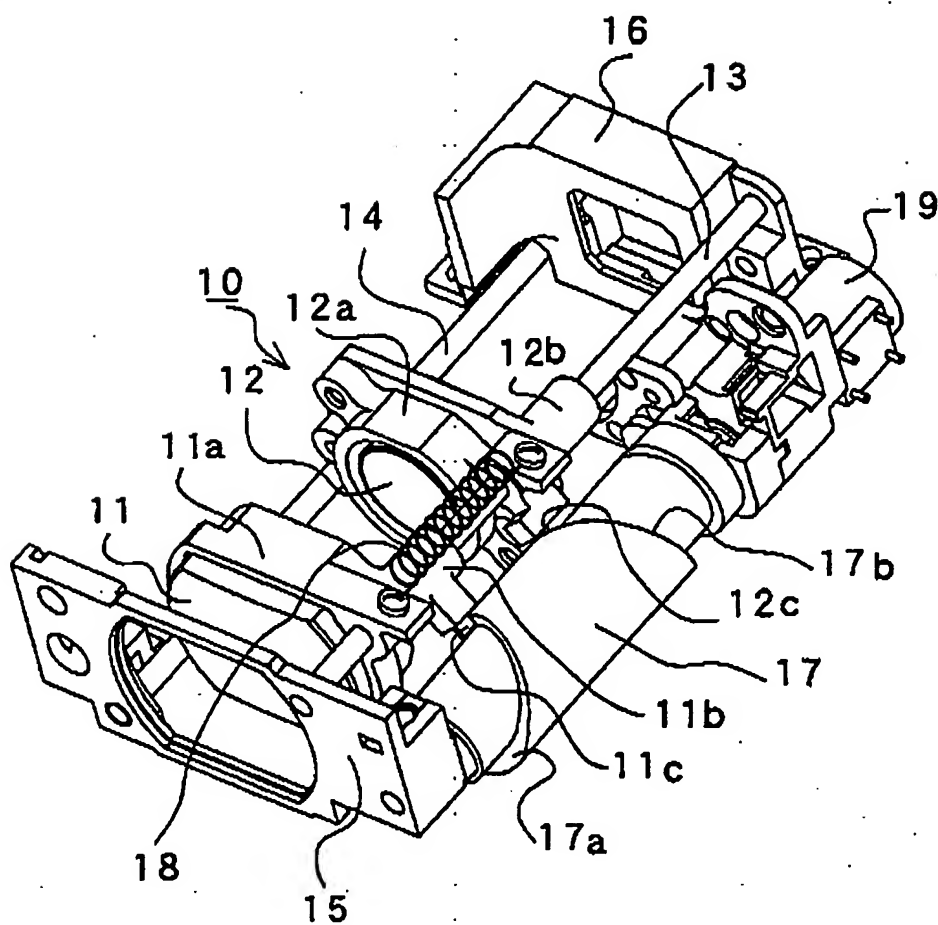
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FIG.44



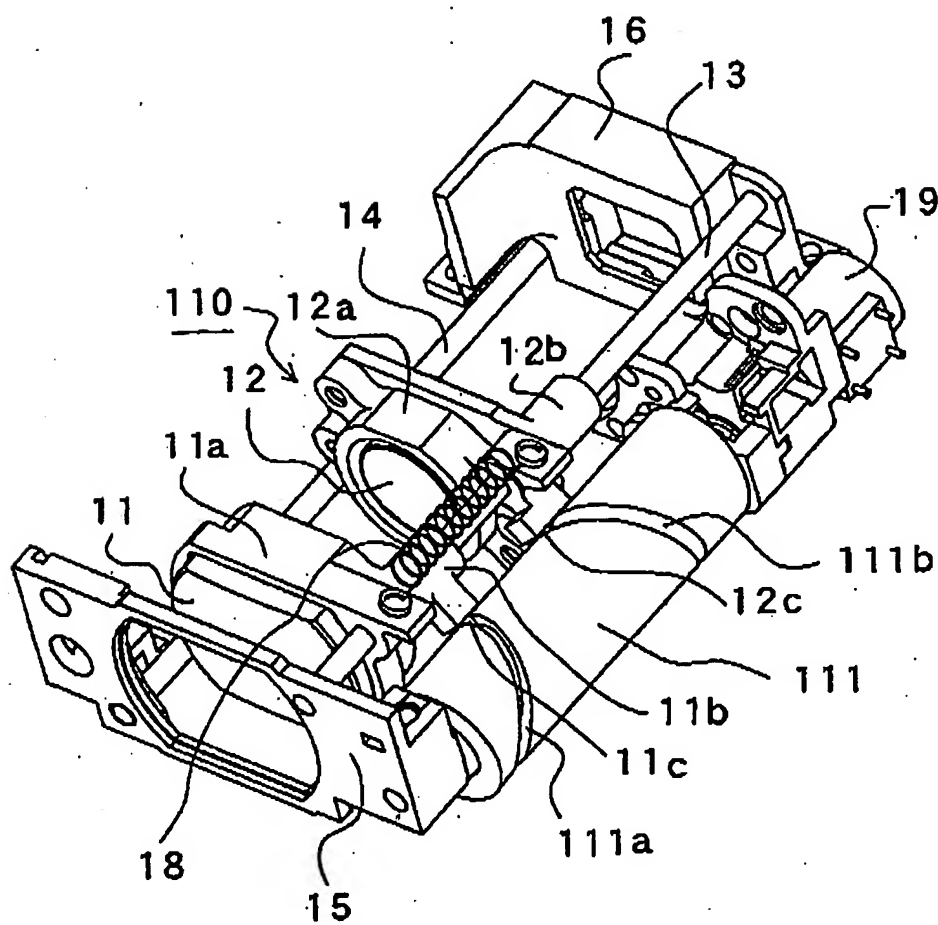
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FIG.45



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FIG.46





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FIG.47

